ABSTRACT

Architecture of an encryption circuit (1) simultaneously processing various encryption algorithms, the circuit being capable of being coupled with a host system (HS) hosted by a computing machine. The circuit (1) comprises an input/output module (2), responsible for the data exchanges between the host system (HS) and the circuit via a dedicated bus (PCI), an encryption module (3) coupled with the input/output module (2), in charge of the encryption and decryption operations as well as the storage of all of the circuit's sensitive information; and isolation means (4) between the input/output module (2) and the encryption module (3), making the sensitive information stored in the encryption module (3) inaccessible to the host system (HS), and ensuring the parallelism of the operations performed by the input/output module (2) and the encryption module (3).

The applications specifically include the "hardware" protection of computer servers or stations.

ONE FIGURE